

## CLAIMS

What is claimed is:

- 1           1.     An apparatus comprising:  
2           a processor interface unit; and  
3           a cache to store information received from a processor coupled to the processor  
4     interface unit, the cache to store disposable information.
  
- 1           2.     The apparatus of claim 1, the cache to further store non-disposable  
2     information.
  
- 1           3.     The apparatus of claim 2, further comprising a cache management unit to  
2     determine whether a cache entry contains disposable information.
  
- 1           4.     The apparatus of claim 3, further comprising a bus interface unit to allow a  
2     device coupled to the bus interface unit to access the cache.
  
- 1           5.     The apparatus of claim 4, the cache management unit to allow the cache  
2     entry to be overwritten if the device coupled to the bus interface unit reads the cache entry  
3     and if the cache management logic determines that the cache entry contains disposable  
4     information.
  
- 1           6.     The apparatus of claim 5, further comprising a system memory controller.

1           7.       The apparatus of claim 6, the cache management unit to cause the cache  
2 entry contents to be delivered to the system memory controller for delivery to a system  
3 memory if the cache management unit determines that the cache entry does not contain  
4 disposable information.

1           8.       The apparatus of claim 7, the processor interface unit to receive a  
2 disposable information attribute indication from the processor when the processor  
3 delivers disposable information to the processor interface unit.

1           9.       The apparatus of claim 7, the cache management unit to determine  
2 whether the cache entry contains disposable data by comparing the cache entry address  
3 with a range of addresses that define a disposable information address space.

1           10.      The apparatus of claim 9, further comprising at least one programmable  
2 register to store addresses that define a disposable address space.

1           11.      A system, comprising:  
2 a processor; and  
3 a system logic device coupled to the processor, the system logic device including  
4 a processor interface unit, and  
5 a cache to store information received from a processor coupled to the  
6 processor interface unit, the cache to store disposable information.

1           12.    The system of claim 11, the cache to further store non-disposable  
2   information.

1           13.    The system of claim 12, the system logic device further including a cache  
2   management unit to determine whether a cache entry contains disposable information.

1           14.    The system of claim 13, the system logic device further including a bus  
2   interface unit.

1           15.    The system of claim 14, further comprising a device coupled to the system  
2   logic device bus interface unit.

1           16.    The system of claim 15, the cache management unit to allow the cache  
2   entry to be overwritten if the device coupled to the bus interface unit reads the cache entry  
3   and if the cache management logic determines that the cache entry contains disposable  
4   information.

1           17.    The system of claim 16, the system logic device further including a system  
2   memory controller.

1           18.    The system of claim 17, further comprising a system memory coupled to  
2   the system memory controller.

1           19.     The system of claim 18, the cache management unit to cause the cache  
2 entry contents to be delivered to the system memory controller for delivery to the system  
3 memory if the cache management unit determines that the cache entry does not contain  
4 disposable information.

1           20.     The system of claim 19, the processor interface unit to receive a disposable  
2 information attribute indication from the processor when the processor delivers  
3 disposable information to the processor interface unit.

1           21.     The system of claim 19, the cache management unit to determine whether  
2 the cache entry contains disposable data by comparing the cache entry address with a  
3 range of addresses that define a disposable information address space.

1           22.     The system of claim 21, the system logic device further including at least  
2 one programmable register to store addresses that define a disposable address space.

1           23.     A method, comprising:  
2 receiving a line of information from a processor;  
3 storing the line of information in a cache;  
4 determining whether the line of information is disposable; and  
5 writing the line of information to a system memory if the information is not  
6 disposable.

